Remarks

This amendment is in response to the Office Action dated June 18, 2002. Claims 1, 7, 14 and 19 have been amended. Claims 6 and 27-31 have been canceled. New claims 32-37 have been added. Claims 1-5, 7-26 and 32-37 are currently pending. Reexamination and reconsideration are respectfully requested.

As requested by the Examiner, applicant affirms the election of Group I, claims 1-26.

Claims 19-23 were rejected under 35 U.S.C. 102(b) as unpatentable over U.S. Patent No. 6,087,243 to Wang. The rejection is respectfully traversed. Applicant respectfully submits that the Examiner cited no portion of the art describing or suggesting a method including "heating the dielectric layer to a temperature of at least 1050°C; and after the heating the dielectric layer to a temperature of at least 1050°C, forming a well in the semiconductor substrate adjacent to the trench" as recited in claim 19, as amended. It appears that Wang, at col. 6, lines 55-59, describes forming well implants and then, after forming the well implants, heating to densify the oxide trench fill. Thus, Wang appears to teach away from claim 19, which recites in part "heating the dielectric layer . . .; and after the heating . . ., forming a well . . ." Accordingly, the rejection of claim 19 should be withdrawn. Claims 20-23 depend from claim 19 and are patentable for at least the same reasons as claim 19.

Claims 1-10 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 6,165854 to Wu. The rejection is respectfully traversed. Applicant respectfully submits that the Examiner cited no portion of the art describing or suggesting a method including "(c) conducting a thermal treatment of the dielectric layer, wherein the thermal treatment is conducted at temperatures of at least 1050°C; and (d) forming a well in the semiconductor layer, and the step (c) is conducted before the step (d)" as recited in claim 1, as amended. Applicant notes that claim 1 was amended to be like original dependent claim 6 written in independent form. The Examiner stated at page 5 of the Office Action that "Wu does not teach forming a well after the conducting a thermal treatment. The order of forming the well and conducting a thermal treatment is seen as a matter of obvious design choice." Applicant submits that the Examiner has provided no support for the contention regarding the forming of the well and the thermal treatment. In fact, the art teaches away from claim 1. For example, as noted above, it appears

that Wang, at col. 6, lines 55-59, describes forming well implants and then, after forming the well implants, heating the oxide trench fill. Thus, the art appears to teach away from claim 1, which recites in part "(c) conducting a thermal treatment of the dielectric layer . . .(d) forming a well in the semiconductor layer, and the step (c) is conducted before the step (d)." Accordingly, the rejection of claim 1 should be withdrawn. Claims 2-10 depend from claim 1 and are patentable for at least the same reasons.

Applicant also notes that claim 7, as amended, recites in part "thermally oxidizing the sidewall surfaces and the bottom surface of the trench to form a thermal oxide layer thereon, wherein the dielectric layer is formed in direct contact with the thermal oxide layer." The Examiner cited no portion of Wu describing such a structure. Wu, at col. 4, lines 14-16, describes depositing a silicon oxynitride film 12 over the thermal oxide 10 and the silicon oxynitride 12 separates the thermal oxide 10 from the CVD oxide trench fill layer 14. Accordingly, at least for the additional reasons above, claim 7 is patentable over Wu. Claims 8-10 depend from claim 7,which depends from claim 1, and are patentable for at least the same reasons as claim 1 and claim 7.

Claims 11-13 were rejected under 35 U.S.C. 103(a) as unpatentable over Wu in view of Wang. Claims 11- 13 depend from claim 1 and as described earlier, Wang teaches away from the method of claim 1. Accordingly, for at least the same reasons as claim 1, claims 11-13 are in patentable form.

Claims 14-18 and 24-26 were rejected under U.S.C. 103(a) as unpatentable over Wang. The rejection is respectfully traversed. Claim 14 recites in part "forming a well in the semiconductor layer adjacent to the trench after the heating the dielectric layer at a temperature of at least 1050°C." For similar reasons as claim 19 as discussed earlier, Wang appears to teach away from the method of claim 14. Accordingly, claim 14 and its dependent claims 15-18 are in patentable form. Claims 24-26 depend from claim 19 and are patentable for at least the same reasons as claim 19 as discussed earlier.

New claims 32-37 have been added. Support for these claims may be found throughout the specification and the original claims. It is believed that no new matter has been entered. Examiner of the new claims is respectfully requested.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 1-5, 7-26 and 32-37 are in patentable form. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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Alan S. Raynes — **Dec. 17 , 2002**
Alan S. Raynes **(Date)**

Version With Markings to Show Changes Made

Claims 1, 7, 14 and 19 were amended as follows:

1. (amended) A method for manufacturing a semiconductor device having a trench isolation region, the method comprising the steps of:

(a) forming a trench in a semiconductor layer;

(b) forming a dielectric layer that fills the trench;

(c) conducting a thermal treatment of the dielectric layer, wherein the thermal treatment is conducted at temperatures of at least 1050°C; and

(d) forming a well in the semiconductor layer, and the step (c) is conducted before the step (d).

7. (amended) A method for manufacturing a semiconductor device having a trench isolation region according to claim 1, wherein the trench includes sidewall surfaces and a bottom surface, the method further comprising of thermally oxidizing the sidewall surfaces and the bottom surface of the trench to form a thermal oxide layer thereon, wherein the dielectric layer is formed in direct contact with the thermal oxide layer layer.

14. (amended) A method for manufacturing a semiconductor device having a trench isolation region, the method comprising:

forming a trench in a semiconductor layer;

forming a dielectric layer in the trench; [and]

heating the dielectric layer at a temperature of at least 1050°C; and

forming a well in the semiconductor layer adjacent to the trench after the heating the dielectric layer at a temperature of at least 1050°C.

19. (amended) A method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

forming a first layer on a semiconductor substrate;

forming a polishing stopper layer above the first layer;

forming at least one trench by etching the first layer while using the polishing stopper layer as a mask;

forming a dielectric layer in and above the trench; [and]

planarizing the dielectric layer using the polishing stopper layer as a stopper;

heating the dielectric layer to a temperature of at least 1050°C; and

after the heating the dielectric layer to a temperature of at least 1050°C, forming a well in the semiconductor substrate adjacent to the trench.